TS4657

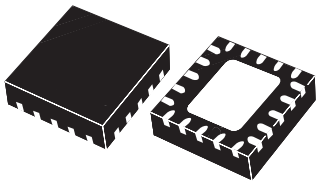
Single supply stereo digital audio line driver with 2.2 Vrms capless outputs

Features

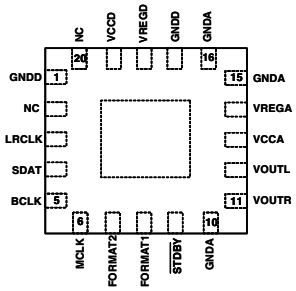
- Single 3.0 to 5.5 V supply for DAC and line driver
- Audio line output: 2.2 Vrms for all V_{CC} range
- 16- to 24-bit audio data format stereo DAC, 32 to 48 kHz sample rate
- I²S, right- or left-justified compatible digital audio interface
- 95 dB SNR A-weighted at 48 kHz, V_{CC} =5 V
- 7.4 mA current consumption at V_{CC} = 3.0 V, full operation
- Internal negative power supply to ensure ground-referenced, capless outputs
- No external capacitor needed for the negative power supply generation
- Integrated structure to suppress pop and click noise
- Available in thin QFN20 4 mm x 4 mm package

Applications

- Digital set-top boxes
- DVD players
- Digital TVs
- Notebooks
- Portable audio equipment
- Sound cards



Pin connections (top view)



Description

The TS4657 is a stereo DAC that integrates a high-performance audio line driver capable of generating a 2.2 Vrms output level from a single 3.0 to 5.5 V supply.

One single supply is sufficient for the digital and analog parts of the circuit, thus eliminating the need for external regulators.

The TS4657 is a low-power consumption device. It features only 22 mW power dissipation at a 3.0 V power supply in full operation.

A 16-bit multi-bit sigma delta DAC is used, operating at 256xFs with oversampling digital interpolation filters. The digital audio data can be 16-to 24-bit long and sample rates from 32 to 48 kHz are supported.

The output stage signal is ground-referenced by using an internal self-generated negative power supply, and as such external bulky output coupling capacitors are not necessary.

The TS4657 is packaged in a small 4 x 4 mm QFN20 package, ideal for portable applications.

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1 Block diagram and pin description

Figure 1. Block diagram

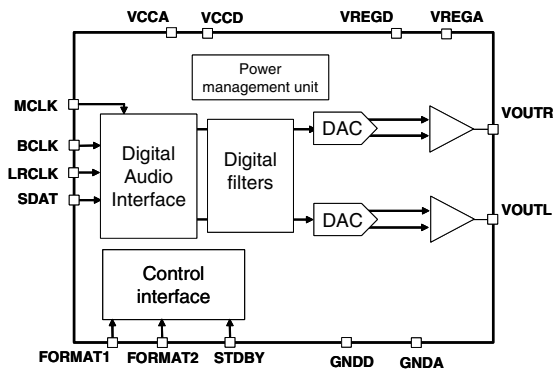


Table 1. Pin description

Pin name	Pin	I/O	Function
GNDD	1	Supply	Digital ground, connected to GND
NC	2	Non-connected pin	This pin must remain non-connected.
LRCLK	3	Digital input	Channel select clock input
SDAT	4	Digital input	Serial audio data input
BCLK	5	Digital input	Bit clock input
MCLK	6	Digital input	Master clock input
FORMAT2	7	Digital input	Selection of the digital data audio format.
FORMAT1	8	Digital input	Selection of the digital data audio format.
$\overline{\text{STDBY}}$	9	Digital input	Input for Standby pin. $\overline{\text{STDBY}}$=VIL: the TS4657 is in shutdown mode.
GNDA	10	Supply	Analog ground, connect to GND.
VOUTR	11	Analog output	Right channel analog output
VOUTL	12	Analog output	Left channel analog output
VCCA	13	Supply	Main analog power supply, connected to VCCD
VREGA	14	Supply	Decoupling pin for the analog part
GNDA	15	Supply	Analog ground, connected to GND
GNDA	16	Supply	Analog ground, connect to GND
GNDD	17	Supply	Digital ground, connected to GND
VREGD	18	Supply	Decoupling pin for the digital part
VCCD	19	Supply	Main digital power supply. Connect to VCCA
NC	20	Non-connected pin	This pin must remain non-connected.

Figure 2. Typical application schematics

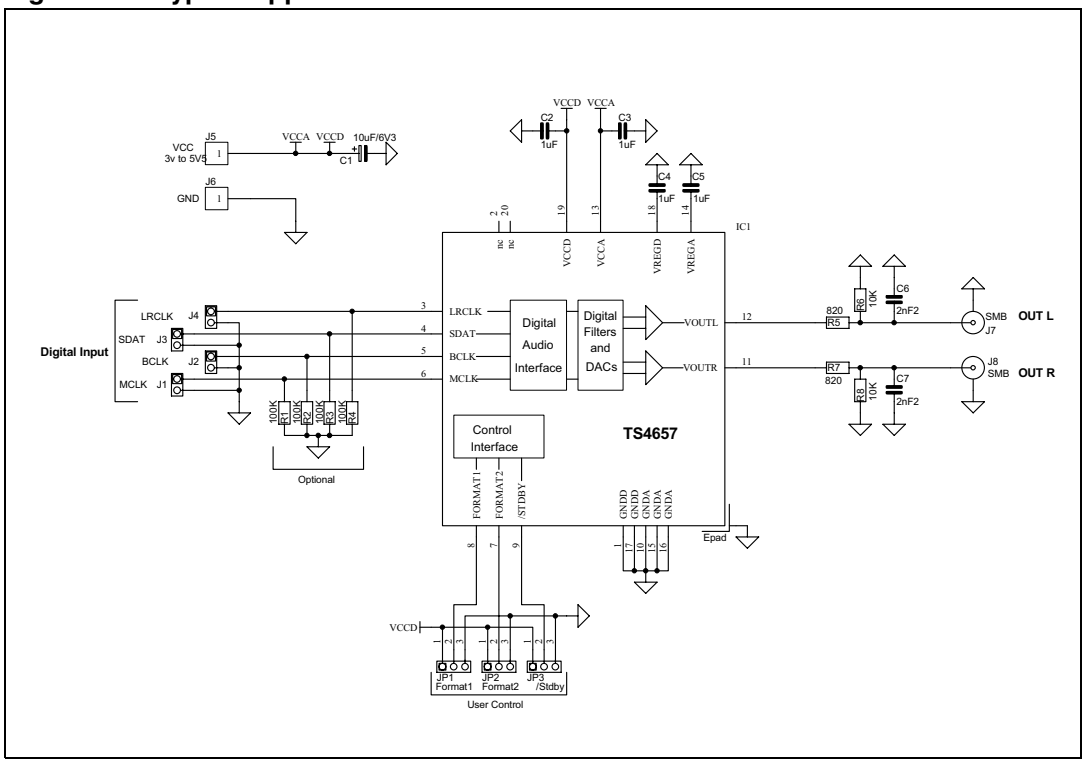
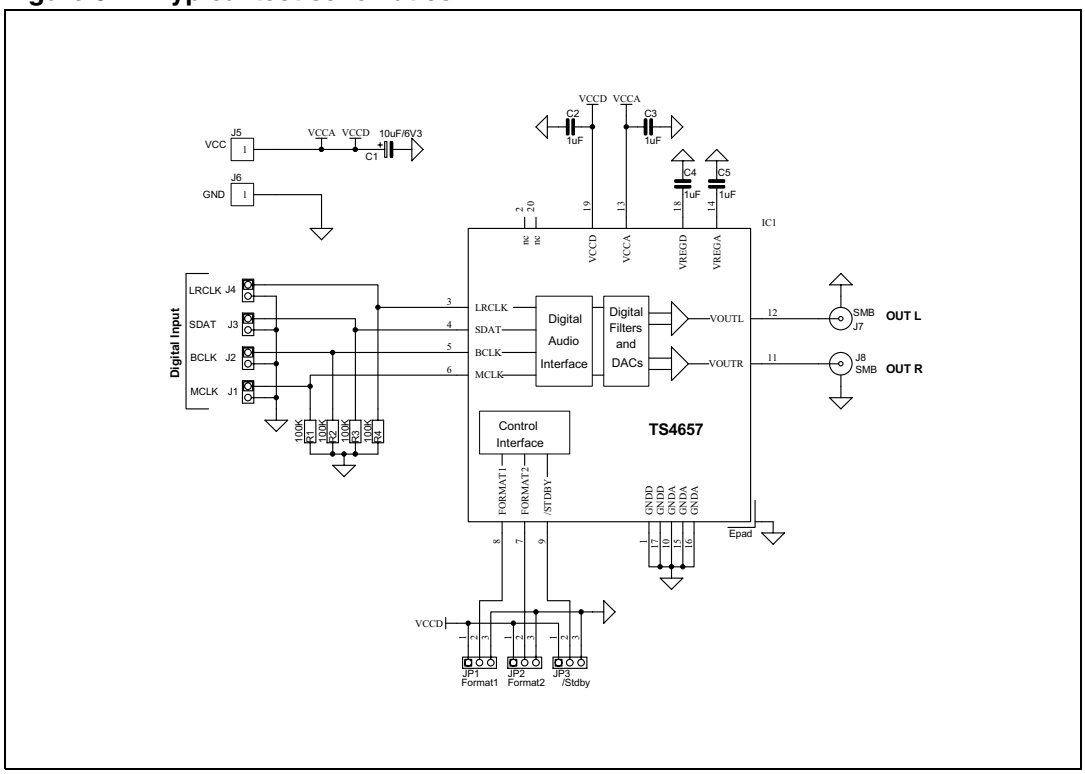


Figure 3. Typical test schematics



2 Absolute maximum ratings

Table 2. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	5.5	V
V_i	Digital input voltage MCLK, BCLK, LRCLK, SDAT, FORMAT1, FORMAT2, STDBY	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient	100	°C/W
ESD	Human body model	2	kV
ESD	Machine model	200	V
	Latch-up immunity	Class A	
	Lead temperature (soldering, 10 secs)	260	°C

1. All voltage values are measured with respect to ground.

3 Electrical characteristics

3.1 Power characteristics

Table 3. VCC = 3.3 V T = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power supply	3.0		5.5	V
I_{CC}	Total supply current. Full operation, R_L = 10 KΩ, vstdby ≥ 2.0 V V_{CC} = 3.0 V V_{CC} = 5.0 V		 7.4 8	 9.5 9.8	mA
I_{CCstby}	Standby current consumption. V_{CC} = 3 V to V_{CC} = 5.5 V Vstdby = 0 V Vstdby = 0.8 V		 25 50	 1000 2000	nA

3.2 Package thermal characteristics

Table 4. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{thja}	Thermal resistance junction to ambient for QFN20(1)		40		°C/W

1. With heat sink surface = 125 mm^2.

3.3 DAC and output stage performances

Table 5. V_{CC} = 3.0 V to Vcc = 5.5 V, Rload = 10 kΩ Cload = 100 pF, T = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Operating conditions					
-	Audio data input format	16		24	bits
Fs	Sampling frequency	32		48	kHz
R_L	Load resistor	5	10		kΩ
C_L	Load capacitance		100	150	pF
Digital input characteristics					
VIL	Low-level input voltage			0.8	V
VIH	High-level input voltage	2			V
Dynamic parameters					
VoutRMS	Full-scale output voltage swing V_{in} at 0 dBFS; $R_L \geq R_L$min; C_L=100 pF	2.1	2.2		Vrms

Table 6. V_{CC} = 3.3 V, Rload = 10 kΩ Cload = 100 pF, T = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Dynamic parameters					
DR	Dynamic range. A-weighted 16-bit data; V_{in} at -60 dBFS, F_S = 48 kHz, F_{in} = 1 kHz	88	93		dB
SNR	Signal-to-noise ratio, F_S = 48 kHz, F_{in} = 1 kHz, referred to output V_{in} at -6 dBFS; A-weighted, 18-bit data input V_{in} at -6 dBFS; unweighted, 18-bit data input V_{in} at 0 dBFS; A-weighted, 16-bit data input	 89 87 87	 94.5 92.5 93		dB
THD+N	Total harmonic distortion and noise. Fin = 1 kHz V_{in} at -20 dBFS, 18-bit data input V_{in} at -6 dBFS, 18-bit data input V_{in} at 0 dBFS, 16-bit data input	 74	 72 82 81		dB
PSRR	Power supply rejection ratio, Vripple = 200 mVpp F= 217 Hz F= 1 kHz 20 Hz < F < 20 kHz		 80 71 46		dB
LRiso	Channel separation. 1 kHz, V_{in} at 0 dBFS		100		dB
V_{oo}	Output offset voltage	-20		20	mV
	Gain channel balance	-0.2	0.01	0.2	dB
t_{wu}	Wake-up time		4.5		ms

Table 7. V_{CC} = 5 V, Rload = 10 kΩ, Cload = 100 pF, T = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DR	Dynamic range; A-weighted 16-bit data; measured at -60 dBFS, F_S = 48 kHz, F_{in} = 1 kHz	88	93		dB
SNR	Signal-to-noise ratio, F_S = 48 kHz, F_{in} = 1 kHz, referred to output V_{in} at -6 dBFS; A-weighted, 18-bit data input V_{in} at -6 dBFS; unweighted, 18-bit data input V_{in} at 0 dBFS; A-weighted, 16-bit data input	89	95 93 93		dB
THD+N	Total harmonic distortion and noise. Fin = 1 kHz V_{in} at -20 dBFS V_{in} at -6 dBFS V_{in} at 0 dBFS	74	72 82.5 81.5		dB
PSRR	Power supply rejection ratio, Vripple = 200 mVpp F= 217 Hz F= 1 kHz 20 Hz < F < 20 kHz		80 73 48		dB
LRiso	Channel separation. 1 kHz, Vin at 0 dBFS		100		dB
V_{oo}	Output offset voltage	-20		20	mV
	Gain channel balance	-0.2	0.01	0.2	dB
t_{wu}	Wake-up time(1)	3	4.5	6	ms

1. See timing diagram in application information.

3.3.1 Terminology

SNR: signal-to-noise ratio is expressed in dB. The theoretical formula is:

$$SNR_{dB} = 10\log\left(\frac{VH_1^{\,2}}{V_{noise}^{\,2}}\right)$$

where V_{noise} is the integrated noise from 20 Hz to 20 kHz and VH_1 is the fundamental of the signal.

For unweighted measurements, the SNR is given by:

$$SNR_{dB} = 10\log\left[\frac{VH_1^{\,2}}{\int_{20Hz}^{20kHz} \left|u(f)(v_{noise}(f))\right|^2 df}\right]$$

where v_{noise} is the noise spectral density and u(f) is the unweighted filter transfer function (20 Hz, 20 kHz).

For A-weighted measurements:

$$SNR_{dB_A} = 10\log\left[\frac{VH_1^{\,2}}{\int_{20Hz}^{20kHz} \left|A(f)(v_{noise}(f))\right|^2 df}\right]$$

where v_{noise} is the noise spectral density and A(f) is the A-weighted filter transfer function.

THD+N: total harmonic distortion and noise-to signal-ratio is expressed in dB. It is given by:

$$THD + N_{dB} = 10\log\left[\frac{\sum_{i=2}^{k} VH_i^2 + V_{noise}^2}{V_{outrms}^2}\right]$$

where VH_i is the rms value of the harmonic components.

SINAD: signal and noise distortion is expressed in dB. The equation is given by:

$$SINAD_{dB} = 10\log\left[\frac{V_{outrms}^2}{\sum_{i=2}^{k} VH_i^2 + V_{noise}^2}\right]$$

DR: dynamic range is expressed in dB, with the following equation:

$$DR_{dB} = 10\log\left[\frac{\sum_{i=1}^{k} VH_i^2}{V_{noise}^2}\right]$$

3.4 Digital filter characteristics

Table 8. V_{CC} = 3.3 V T= 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
-	Passband edge (-3 dB)		0.48Fs		
-	Passband ripple f < 0.45 Fs			+/- 0.1	dB
-	Stopband attenuation f > 0.55 Fs	-50			dB

3.4.1 DAC digital filter response

Figure 4. DAC digital filter frequency response from 32 to 48 kHz

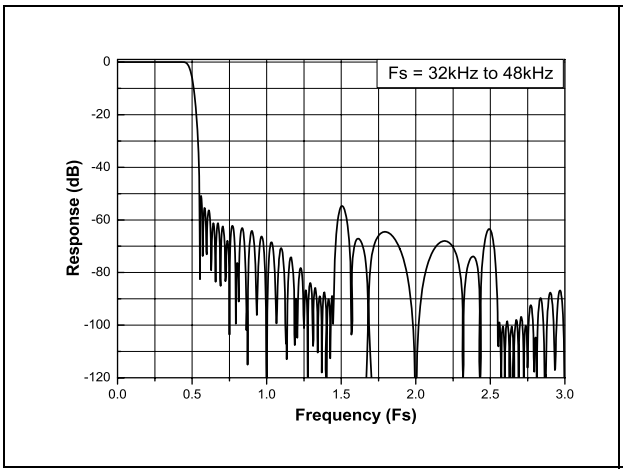


Figure 5. DAC digital filter transition band from 32 to 48 kHz

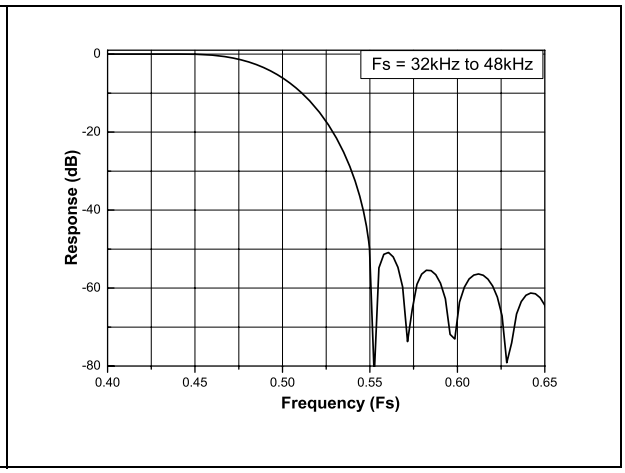
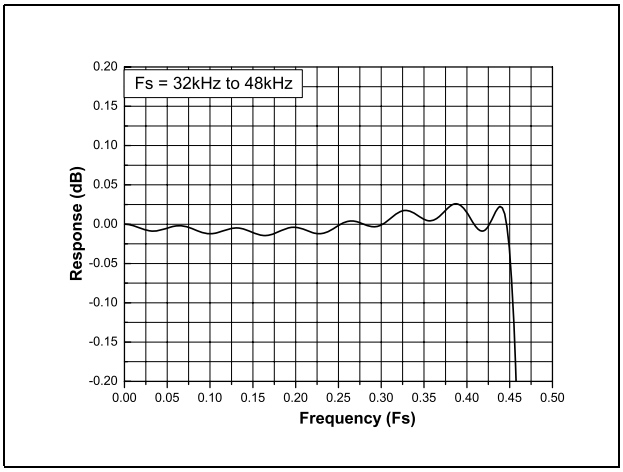


Figure 6. DAC digital filter ripple from 32 to 48 kHz



3.5 Electrical measurement curves

Figure 7. Crosstalk vs. frequency

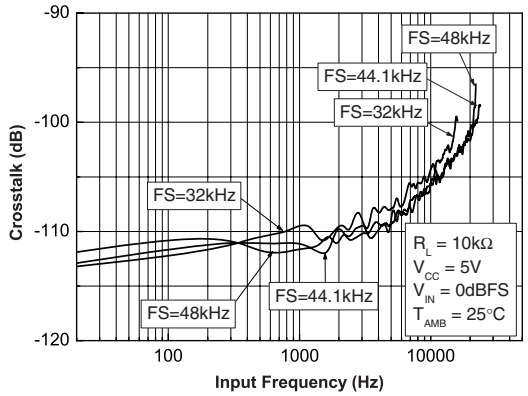


Figure 8. Crosstalk vs. frequency

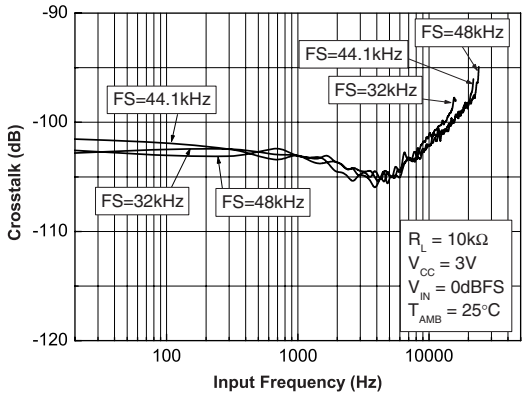


Figure 9. Frequency response

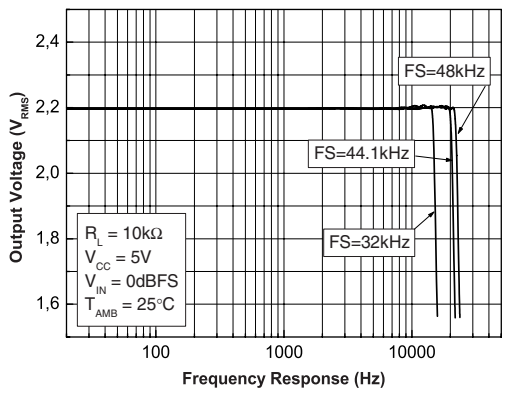


Figure 10. Frequency response

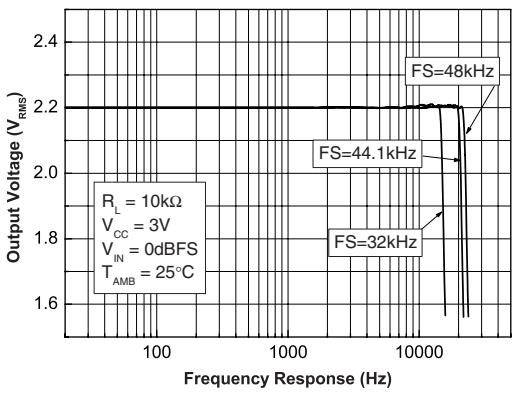


Figure 11. Current consumption vs. power supply voltage

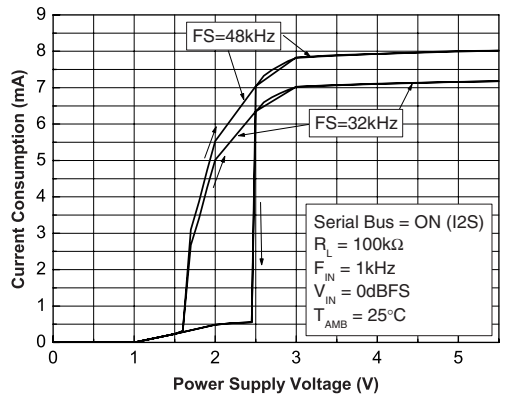


Figure 12. Current consumption vs. standby voltage

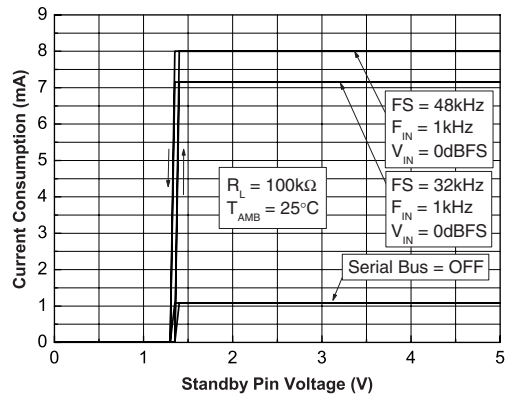


Figure 13. Output swing vs. power supply voltage

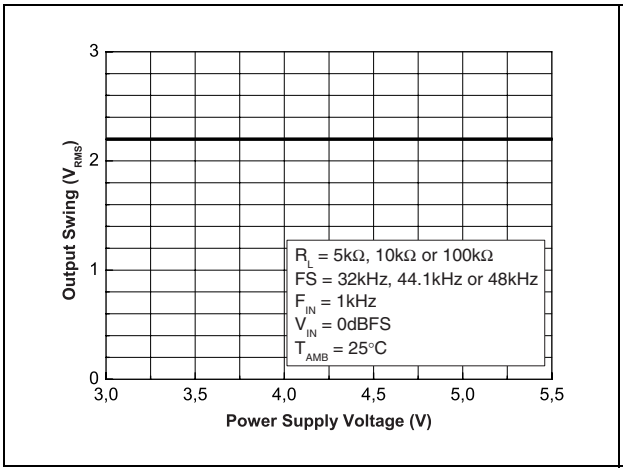


Figure 14. Power dissipation vs. frequency

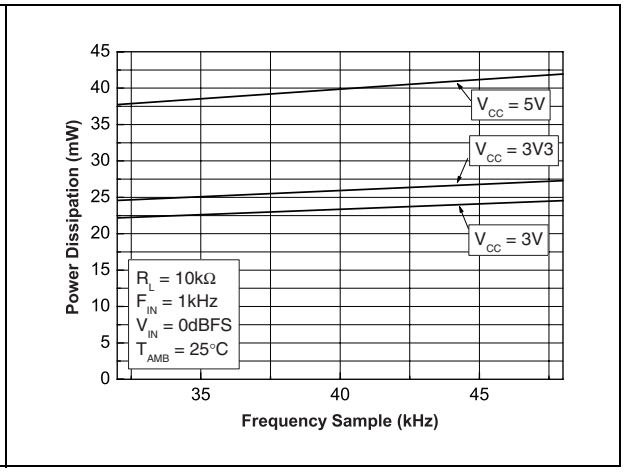


Figure 15. Power supply rejection ratio vs. frequency

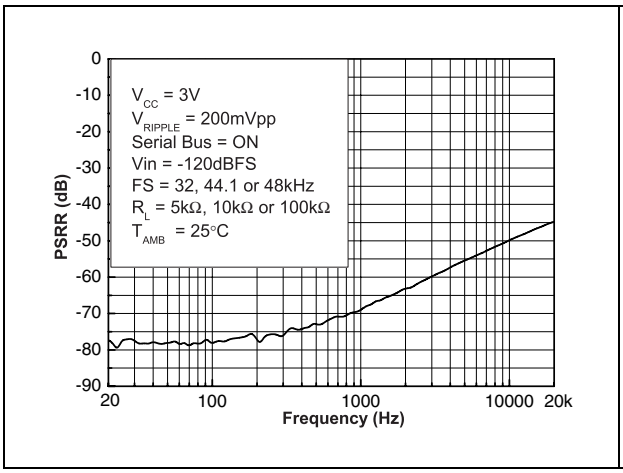


Figure 16. Power supply rejection ratio vs. frequency

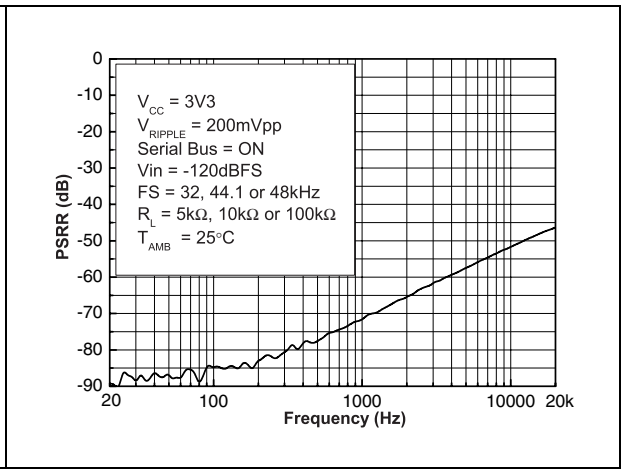


Figure 17. Power supply rejection ratio vs. frequency

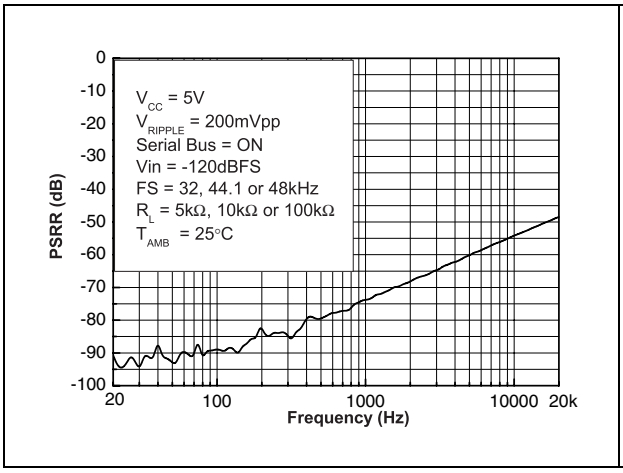


Figure 18. Signal to noise ratio vs. input level

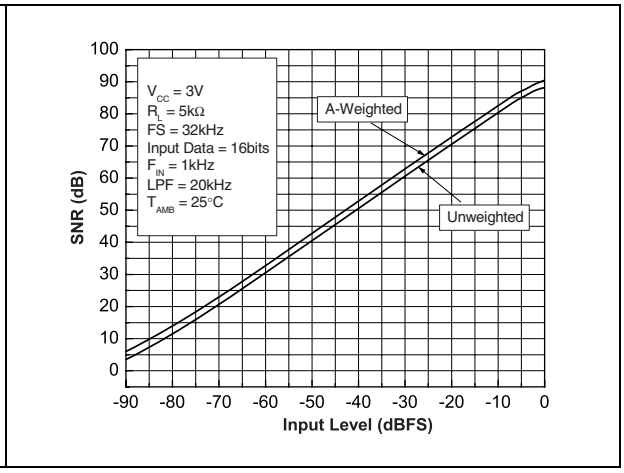


Figure 19. Signal to noise ratio vs. input level

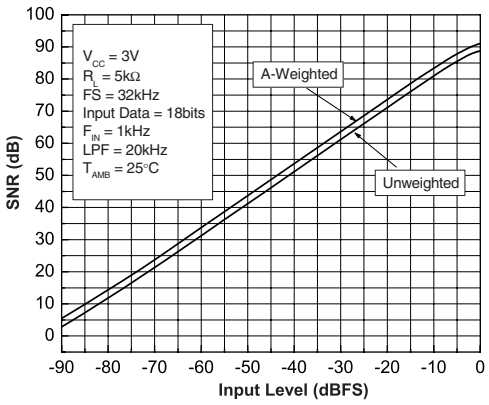


Figure 20. Signal to noise ratio vs. input level

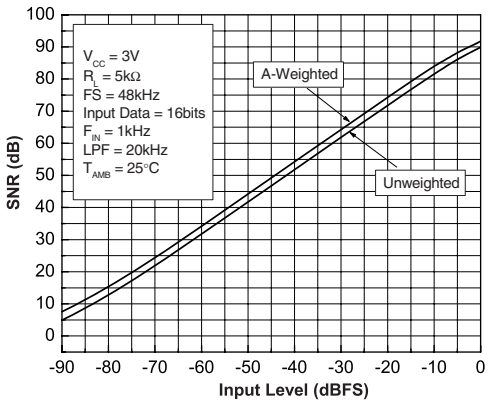


Figure 21. Signal to noise ratio vs. input level

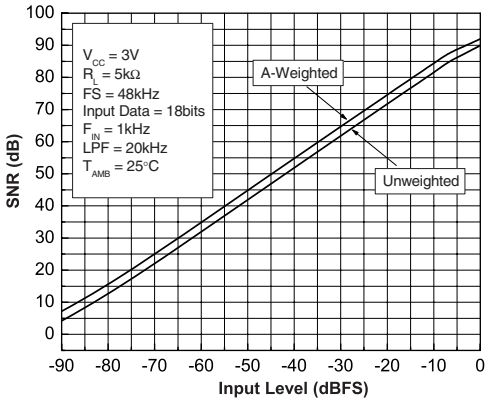


Figure 22. Signal to noise ratio vs. input level

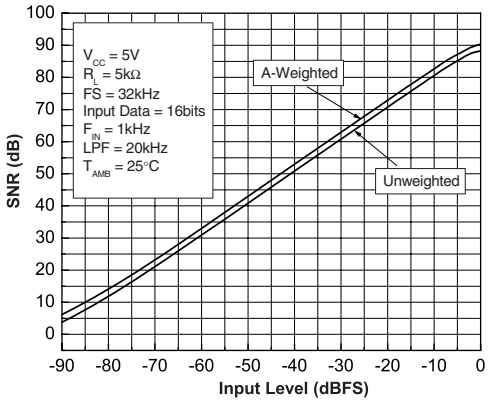


Figure 23. Signal to noise ratio vs. input level

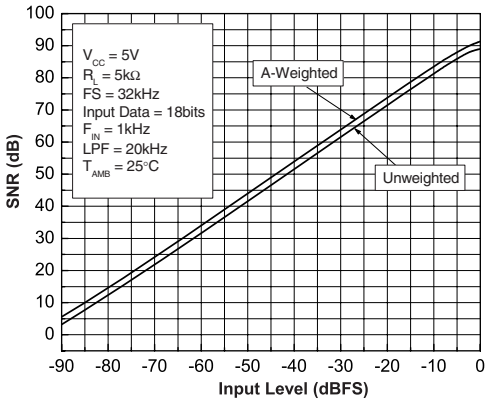


Figure 24. Signal to noise ratio vs. input level

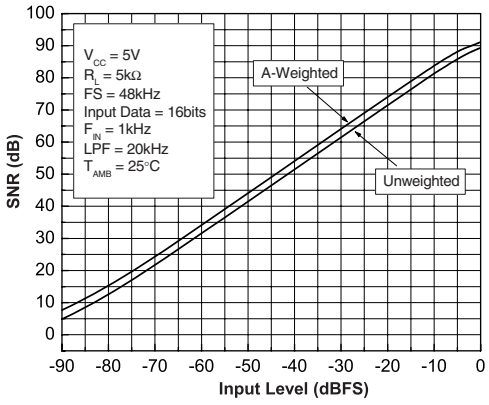


Figure 25. Signal to noise ratio vs. input level

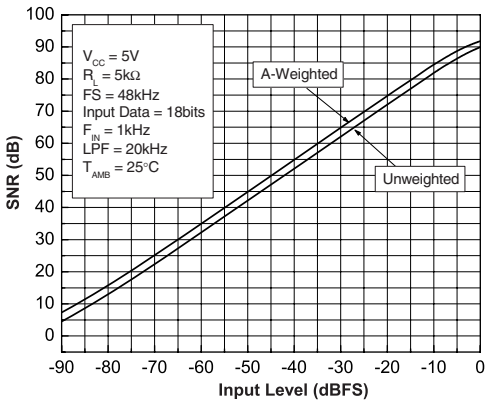


Figure 26. Signal to noise ratio vs. input level

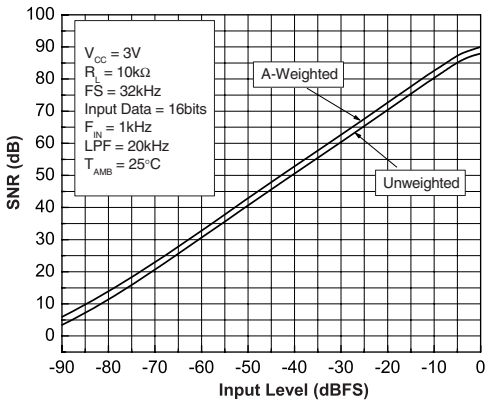


Figure 27. Signal to noise ratio vs. input level

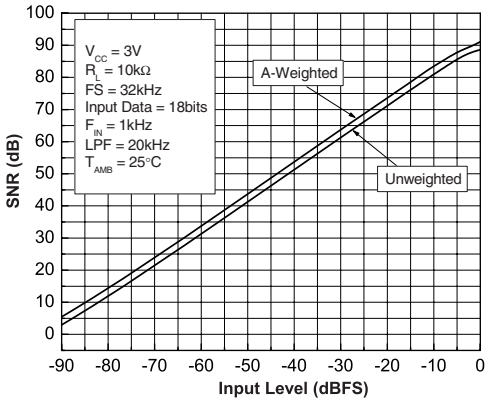


Figure 28. Signal to noise ratio vs. input level

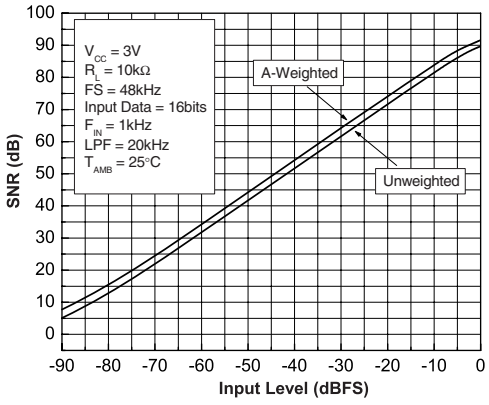


Figure 29. Signal to noise ratio vs. input level

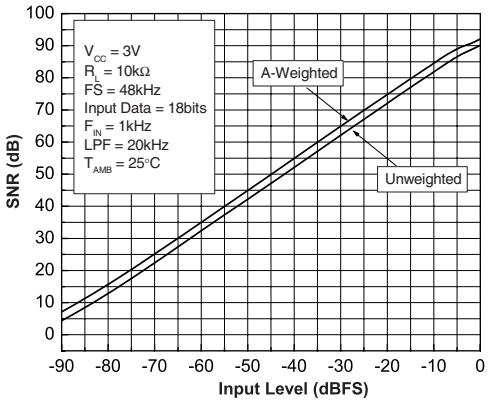


Figure 30. Signal to noise ratio vs. input level

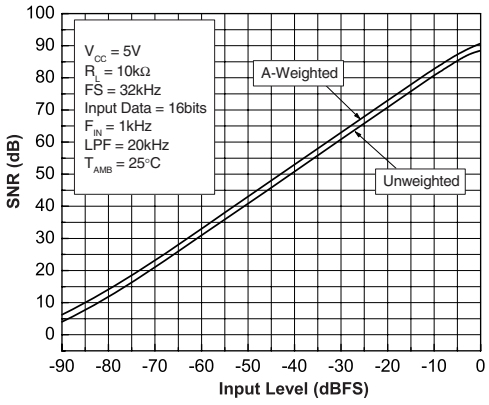


Figure 31. Signal to noise ratio vs. input level

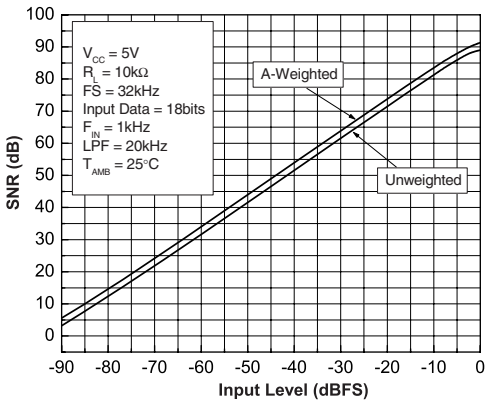


Figure 32. Signal to noise ratio vs. input level

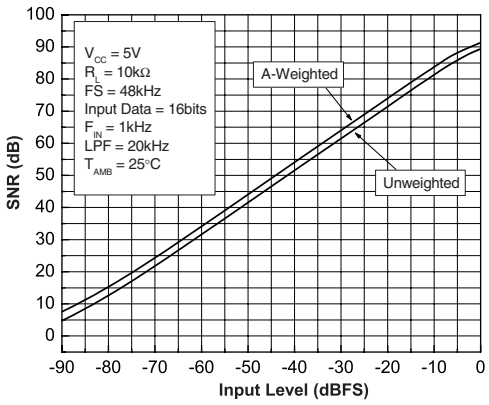


Figure 33. Signal to noise ratio vs. input level

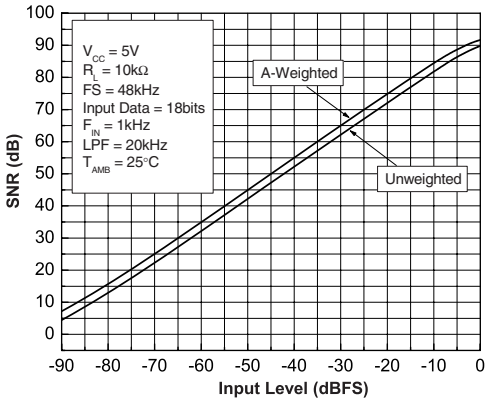


Figure 34. Total harmonic distortion and noise vs. frequency

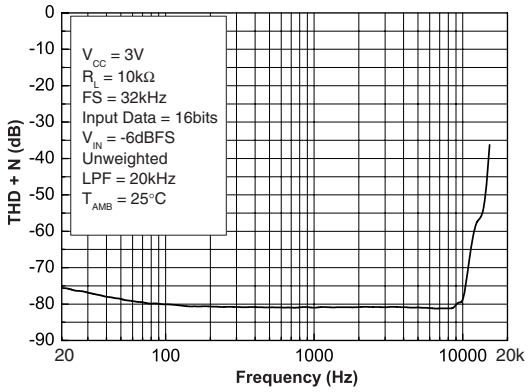


Figure 35. Total harmonic distortion and noise vs. frequency

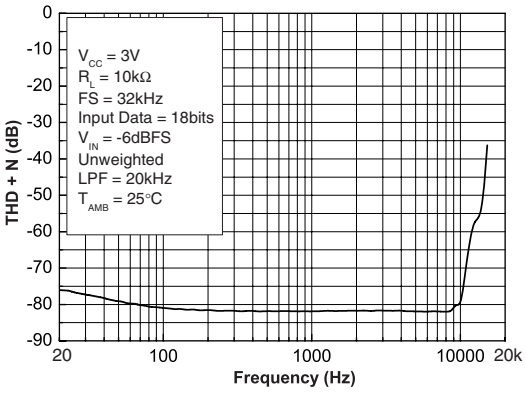


Figure 36. Total harmonic distortion and noise vs. frequency

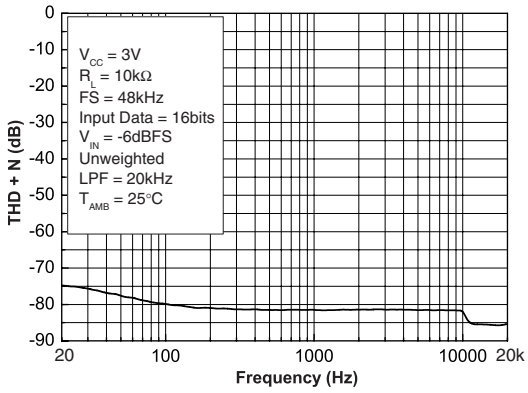


Figure 37. Total harmonic distortion and noise vs. frequency

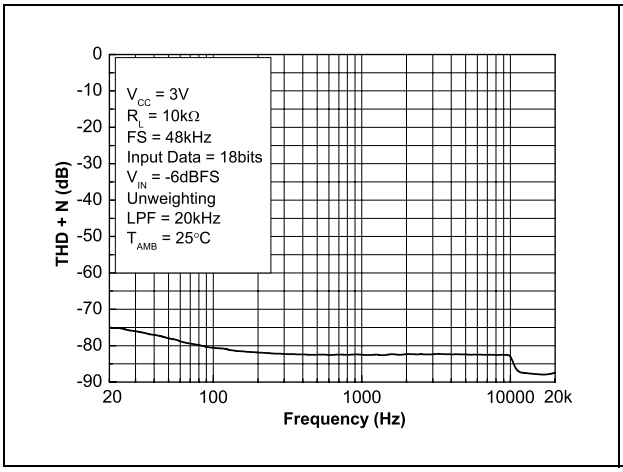


Figure 38. Total harmonic distortion and noise vs. frequency

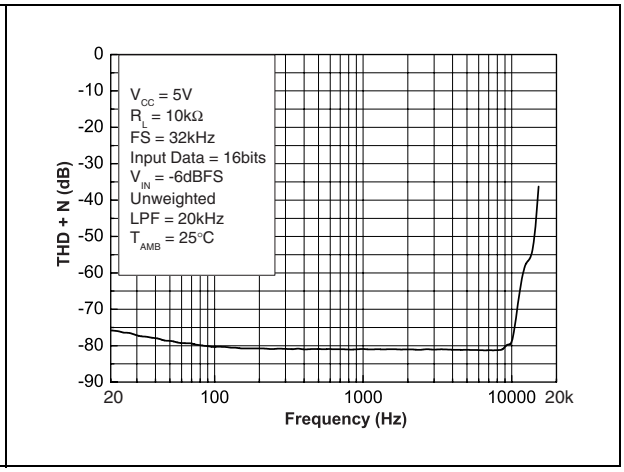


Figure 39. Total harmonic distortion and noise vs. frequency

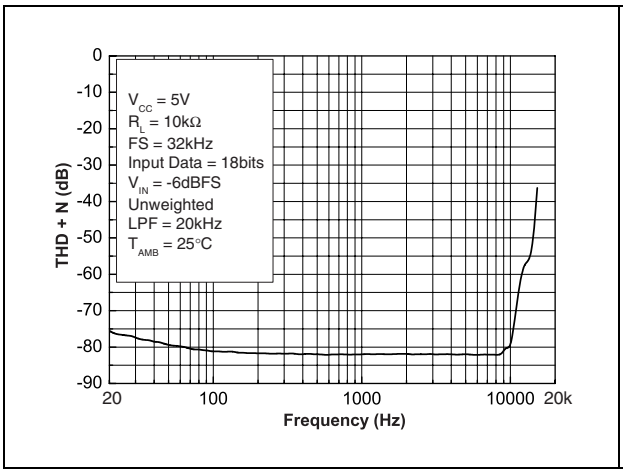


Figure 40. Total harmonic distortion and noise vs. frequency

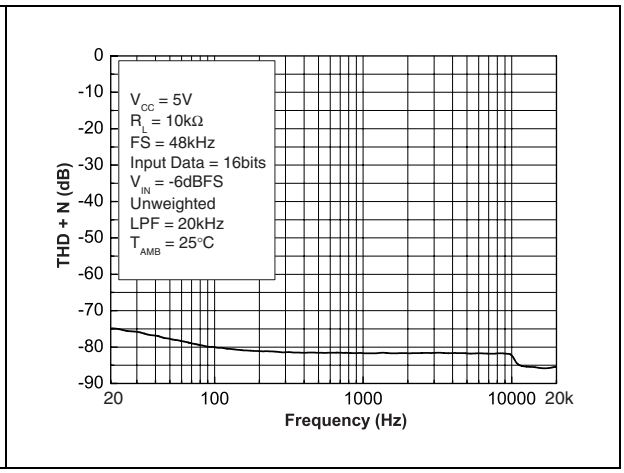


Figure 41. Total harmonic distortion and noise vs. frequency

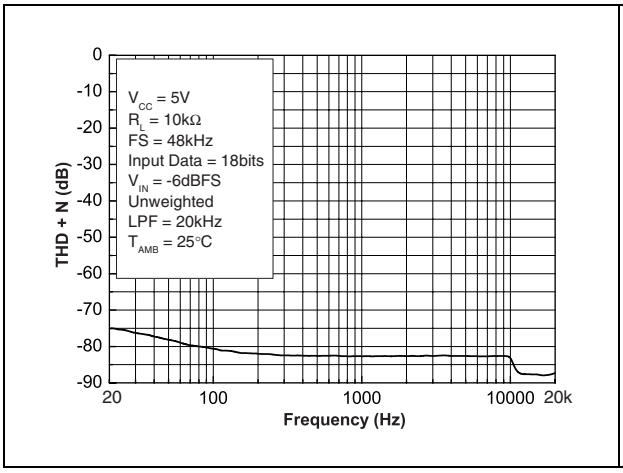


Figure 42. Total harmonic distortion and noise vs. input level

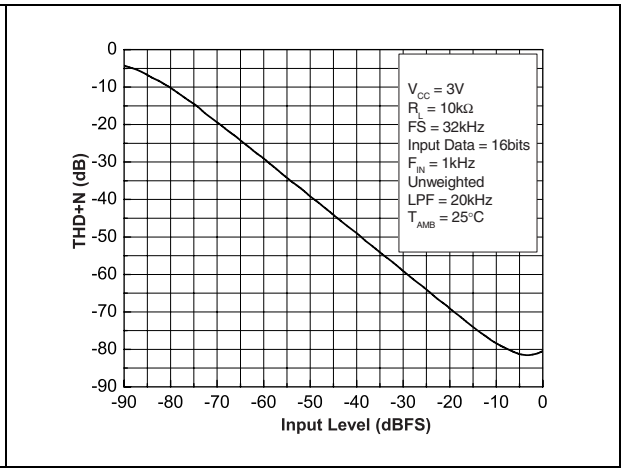


Figure 43. Total harmonic distortion and noise vs. input level

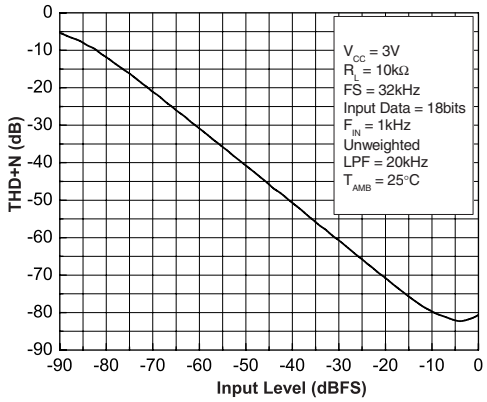


Figure 44. Total harmonic distortion and noise vs. input level

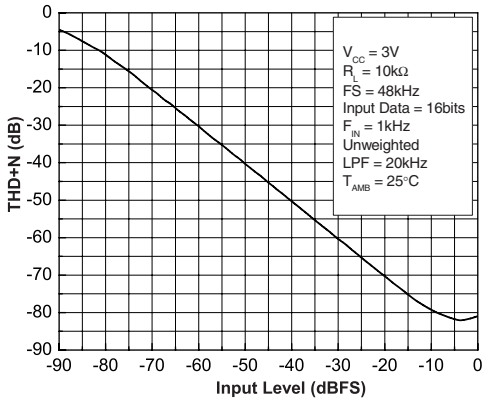


Figure 45. Total harmonic distortion and noise vs. input level

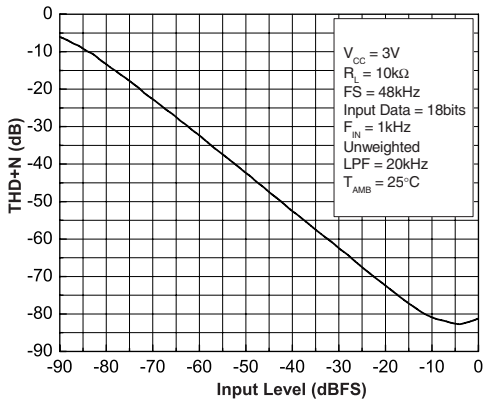


Figure 46. Total harmonic distortion and noise vs. input level

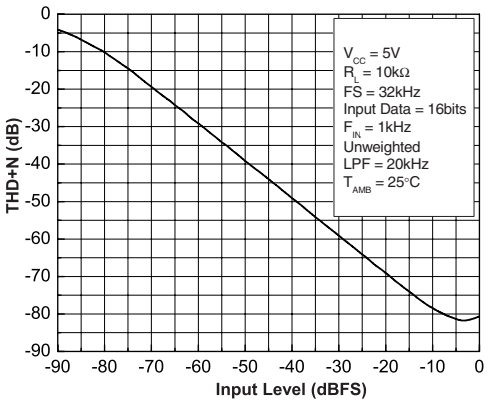


Figure 47. Total harmonic distortion and noise vs. input level

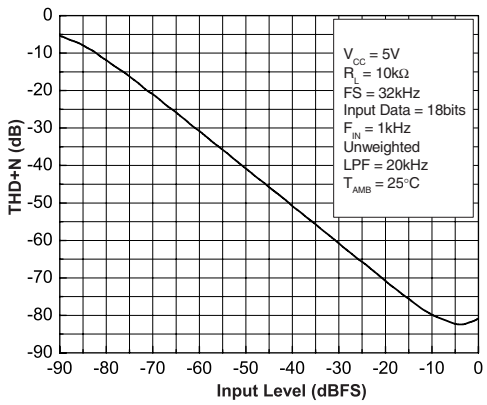


Figure 48. Total harmonic distortion and noise vs. input level

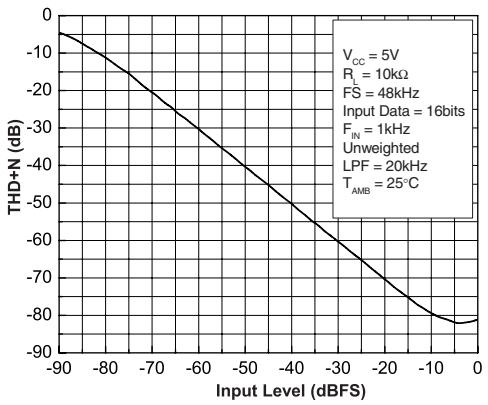
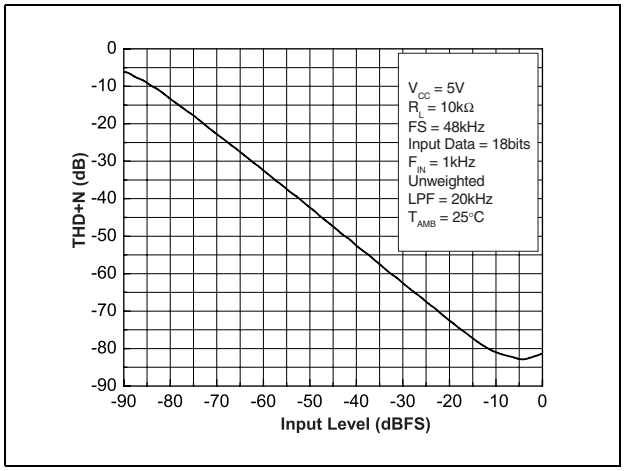


Figure 49. Total harmonic distortion and noise vs. input level



4 Application information

4.1 Serial audio interface

4.1.1 Master clock and data clocks

Three external clock signals are applied to the TS4657. The MCLK is the external master clock applied by the audio data processor. The LRCLK is the channel frequency, also called LEFT/RIGHT clock, at which the digital words for each channel are input to the device. The LRCLK clock is the sample rate of the audio data. The ratio MCLK/LRCLK must be an integer as shown in *Table 9*.

The BCLK is the bit clock and represents the clock at which the audio data is serially shifted into the audio port. BCLK is linked to LRCLK. The minimum required BCLK frequency is twice the audio sample rate times the number of bits in each audio word. Refer to *Table 10* for the BCLK/LRCLK ratio.

MCLK, LRCLK and BCLK must be synchronous clock signals.

Table 9. Audio data sampling rates

LRCLK (kHz)	MCLK (MHz)
	256x
32	8.192
44.1	11.2896
48	12.288

4.1.2 Digital audio input format

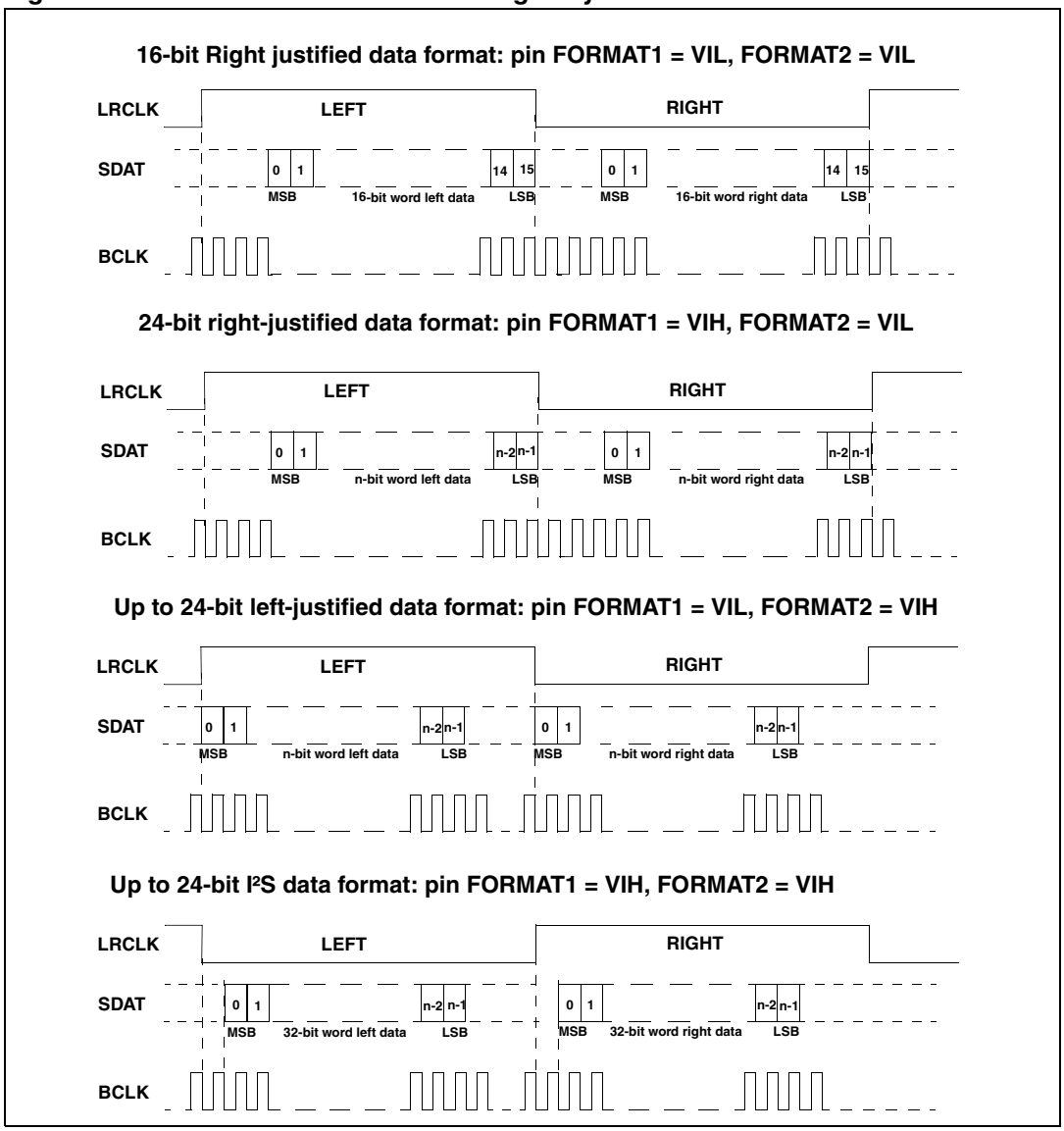
The TS4657 receives serial digital audio data through a 3-wire interface. SDAT is the serial audio data input. The data is entered MSB first and is a two's complement. The data can be I^2S, right or left justified. The data format is chosen with the control pins FORMAT1 and FORMAT2 as detailed in *Table 10*.

Figure 50 on page 20 summarizes the implementation of the audio data format.

Table 10. Digital audio data formats supported by the TS4657

FORMAT2	FORMAT1	Data Format	BCLK/LRCLK ratio	
			Min	Max
0	0	Right-justified, 16-bit data Data valid on rising edge of BCLK	32	256
0	1	Right-justified, 24-bit data Data valid on rising edge of BCLK	48	256
1	0	Left-Justified, 16-bit up to 24-bit data Data valid on rising edge of BCLK	2 x number of bits of data	256
1	1	I^2S, 16-bit up to 24-bit data Data valid on rising edge of BCLK	2 x number of bits of data	256

Figure 50. Audio interface formats managed by the TS4657



4.2 Power-management unit

The TS4657 utilizes a power-management unit to supply its internal structures.

A self-generated negative supply enables the drivers to be powered from positive and negative supplies, therefore increasing the amplitude of the output signal. This internal negative supply switches at a higher frequency than traditional architectures, derived from the master clock MCLK. This structure uses an original design that enables one to suppress the flying or floating capacitors. Therefore, only four small ceramic X5R 10V 1-µF decoupling capacitors are necessary for VCCA/VCCD and VREGA/VREGD.

Furthermore, the self-generated negative supply allows the amplifier outputs to be centered around zero, thus the bulky output coupling capacitors can be removed.

4.3 Recommended power-up and power-down sequences

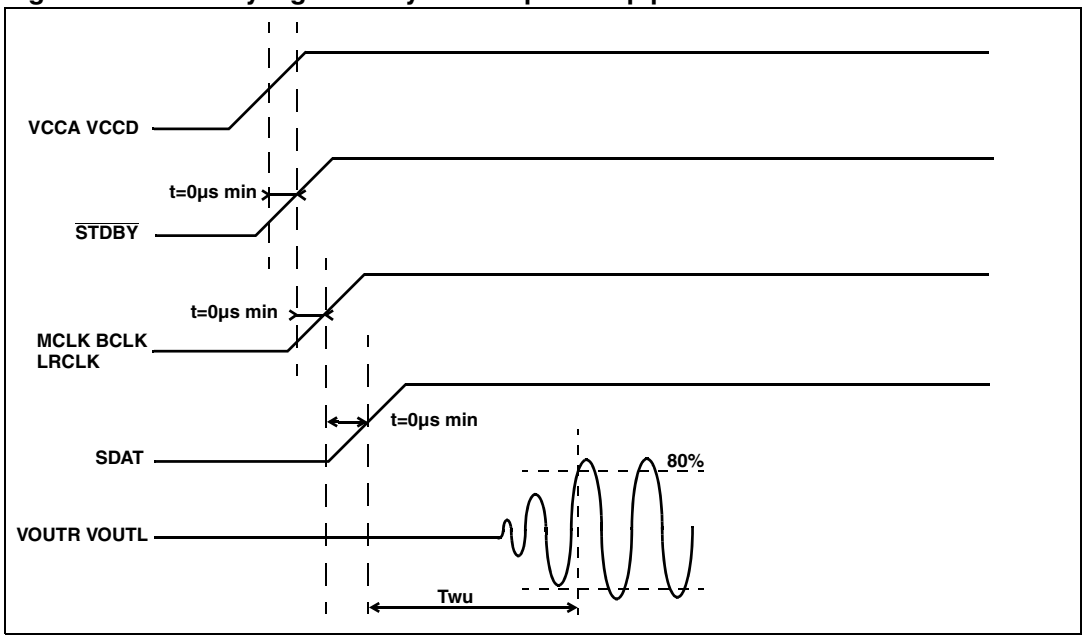
4.3.1 Power-up

It is recommended to power-up the TS4657 prior to applying logical data in order to ensure correct ESD protection biasing.

When the $\overline{\text{STDBY}}$ pin is in a low state (VIL,) the circuit is in standby; when the pin is in a high state (VIH), the circuit is enabled. An internal pull-down resistor will force the $\overline{\text{STDBY}}$ pin to ground if no signal is applied to this pin.

The standby signal can be delayed from the power-up phase but simultaneous stimuli are possible, as shown in *Figure 51*.

Figure 51. Standby signal delayed from power-up phase



The wake-up time (Twu) of the TS4657 is defined as the time between the settlement of the digital input signals STDBY, MCLK, BCLK, LRCLK, SDAT and 80% of the VOUTR/VOUTL amplitude. The Twu of the circuit is typically 4.5 ms.

If all digital input signals are settled and an ON/OFF sequence is applied quickly on the STDBY pin, the internal capacitors remain charged and the Twu is around 1 ms.

4.3.2 Power-down

As described in *Section 4.2*, the MCLK is internally used to supply some blocks. It is therefore recommended not to switch off the MCLK during normal operation.

To properly power-down the device, MCLK, BCLK and LRCLK should be switched off after the STDBY signal.

The power-down time is very short and can be considered as zero.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 QFN20 package information

Figure 52. QFN20 package mechanical drawing

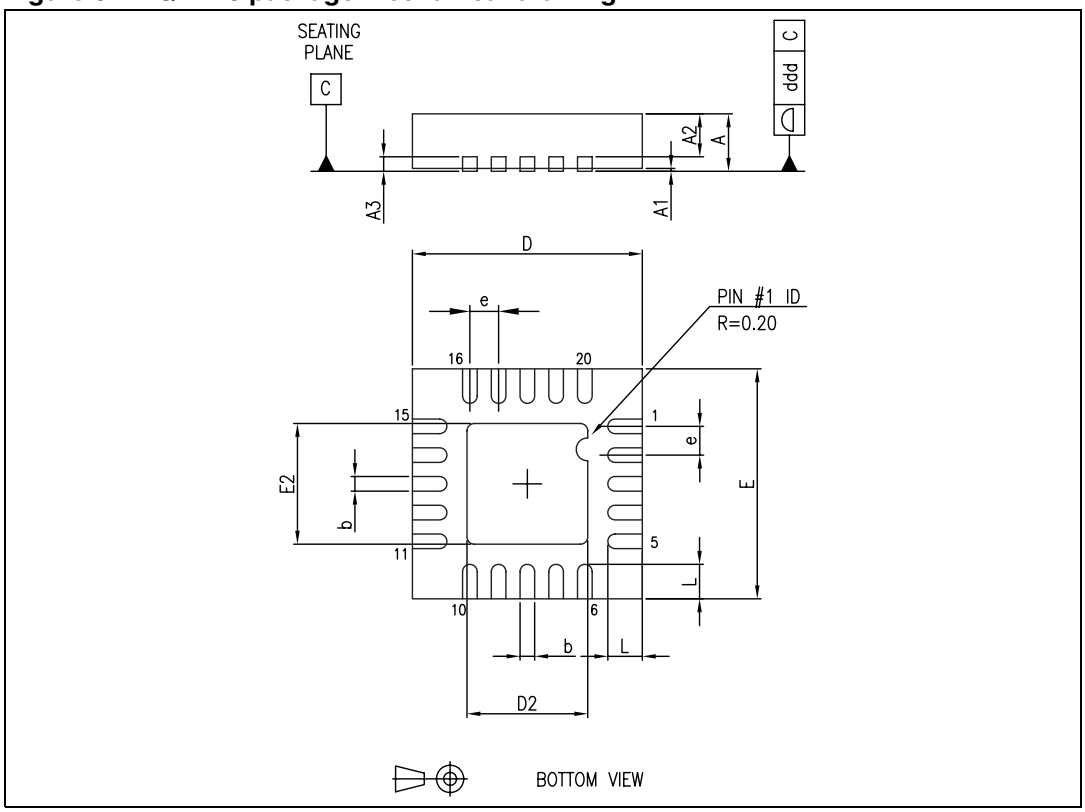


Table 11. QFN20 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.040
A1		0.02	0.05		0.0008	0.002
A2		0.65	1.00		0.026	0.040
A3		0.25			0.010	
b	0.18	0.23	0.30	0.007	0.009	0.012
D	3.85	4.00	4.15	0.152	0.157	0.163
D2	1.95	2.10	2.25	0.077	0.083	0.089
E	3.85	4.00	4.15	0.152	0.157	0.163
E2	1.95	2.10	2.25	0.077	0.083	0.089
e	0.45	0.50	0.55	0.018	0.020	0.022
L	0.35	0.55	0.75	0.014	0.022	0.030
ddd			0.08			0.003

6 Ordering information

Table 12. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4657IQT	-40°C, +85°C	QFN20	Tape & reel	K657

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.

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